IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC. and FAIRCHILD SEMICONDUCTOR CORPORATION, Defendants.	)	**REDACTED PUBLIC VERSION** C.A. No. 04-1371-JJF

DEFENDANTS' ANSWERING BRIEF IN RESPONSE TO PLAINTIFF'S MOTION TO COMPEL PRIVILEGED INFORMATION

Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp. (collectively, "Fairchild") respectfully request that the Court deny as moot Power Integrations' pending motion to compel Fairchild to produce documents and testimony concerning the opinions of Fairchild's counsel.

I. Power Integrations Has Agreed Not To Depose Mr. Schott.

Power Integrations sought to compel the deposition of Mr. Schott – Fairchild's Associate General Counsel.[1] The parties had previously agreed that Fairchild would inform Power Integrations by August 18, 2006 (forty-five days before trial) whether Mr. Schott was expected to testify. Exh. A. Power Integrations agreed that if Mr. Schott was not going to testify, Power Integrations would not depose him. *Id.* On August 11, 2006 (a week before the agreed deadline), Fairchild confirmed that Mr. Schott would not testify. *Id.* Consequently, Power Integrations has now agreed not to depose Mr. Schott. Exh. B. Power Integrations' motion with respect to Mr. Schott is moot.

[1] Mr. Schott received – but was not the Fairchild officer who relied upon –written opinions from Fairchild's outside opinion counsel that the asserted claims are invalid and/or not infringed.

II. The Remaining Issues Are Also Moot.

After the parties agreed that Mr. Schott would not be deposed, Fairchild asked Power Integrations to identify any remaining issues. Exh. A. There were two:

1) "whether REDACTED has any information, from any source, relating to the validity or infringement of the patents [in suit]"; and,

2) "those documents on Fairchild's privilege log which [Power Integrations] identified in [its] letter brief."

Exh. B. Both issues have now been resolved – mooting Power Integrations' motion.

A. Deposition of

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received and relied on the written opinions of Fairchild's outside opinion counsel.[2] Fairchild agrees that there is a limited waiver of the attorney client and work product privileges in light of this reliance. Therefore, while Fairchild will not waive any other applicable privilege on any other subject, Fairchild will permit Power Integrations to depose REDACTED determine whether he has any information, from any source, relating to the validity or infringement of the four asserted patents.

B. Privileged Documents.

Power Integrations identified 35 documents from Fairchild's privilege log that Power Integrations argues relate to the subject of Fairchild's opinion letters – the noninfringement or invalidity of the four asserted patents. DI 307, p. 3. Power Integrations is mistaken – none of these documents relate to those topics in any way. Thus, there is no waiver of any privilege and no obligation to produce these documents.

Power Integrations' document requests were exceedingly broad. Therefore, as Fairchild has explained, Fairchild identified all privileged and potentially responsive documents. Exh. C. Fairchild has never represented that these privileged documents are directly related to Power Integrations or Power Integrations' patents – just that they are potentially responsive to Power

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Integrations' overbroad requests.

The vast majority (31 of the 35) documents identified by Power Integrations have nothing whatsoever to do with the invalidity or non-infringement of the asserted Power Integrations patents. *See* Exh. C. Fairchild assumes that this resolves the issue but will produce the documents *in camera* should the Court wish to inspect them.

Four of the documents identified by Power Integrations mention the asserted patents. *See* Exh. C. While these documents do not directly relate to the noninfringement or invalidity of those patents, to resolve this issue, Fairchild has produced redacted copies of these documents. *Id.* All of the information relating to the asserted patents has, thus, been produced (and only privileged material unrelated to the invalidity or noninfringement of the asserted patents has been redacted). *Id.* Again, Fairchild assumes that this resolves the issue but will provide the documents to the Court in unredacted form should the Court wish to review them *in camera*.

III. Power Integrations Is Not Entitled To Privileged Documents From Fairchild's Litigation Counsel Not Provided To Or Relied Upon By REDACTED

While not clear, Power Integrations may be seeking to impose a privilege waiver so broad that it encompasses documents prepared by Fairchild's outside litigation counsel – the firm of Orrick, Herrington & Sutcliffe (the "Orrick Firm"). Fairchild has not waived its privileges concerning material prepared by the Orrick firm and such documents and information are beyond Power Integrations' discovery.

Fairchild retained outside counsel at the firm REDACTED to analyze Power Integrations' patents and provide written opinions on whether the claims are valid or infringed. REDACTED Fairchild has agreed that Mr. Conrad can be deposed about these opinions and any other opinions he may have received on this subject – the invalidity and noninfringement of the patents-in-suit. Fairchild has never objected to the production of information from REDACTED Indeed, Power Integrations has already received such documents and deposed REDACTED the authors of the opinion letters.

The *EchoStar* case, upon which Power Integrations now relies so heavily only concerned waiver by a company's outside opinion counsel – such as REDACTED here. *EchoStar* does not compel the production of privileged documents from outside litigation counsel – the Orrick Firm – that were not related to the subject of the waiver and were not provided to the reliance witness. To the contrary, *EchoStar* made clear that "work product that was not communicated to [the client] or does not reflect a communication is not within the scope of [the] waiver...." *See In re EchoStar Comm. Corp.* 448 F.3d 1294, 1305 (Fed. Cir. 2006). The Orrick Firm has never provided a willfulness opinion to Fairchild and, in fact, has not provided ***any*** opinions to REDACTED concerning the invalidity or non-infringement of the asserted patents. Therefore, documents prepared by and information received from the Orrick Firm is privileged and that privilege has not been waived.

Power Integrations recognized that there was no broad waiver of documents and information from the Orrick Firm when it agreed not to depose Mr. Schott unless he would be called to testify at trial. This agreement between the parties concerning the scope of the waiver – made before the *EchoStar* case was even decided – must be honored by Power Integrations.

IV. Conclusion.

As set forth above, Power Integrations' pending motion should be denied as moot.

ASHBY & GEDDES

/s/ Tiffany Geyer Lydon

Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Tiffany Geyer Lydon (I.D. #3950)
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Attorneys for Defendants Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corp.

Of Counsel:

ORRICK, HERRINGTON & SUTCLIFFE LLP
G. Hopkins Guy, III
Bas de Blank
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Dated: August 15, 2006

172144.1

EXHIBIT A

REDACTED

EXHIBIT B

FISH & RICHARDSON P.C.

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Date August 11, 2006

To G. Hopkins Guy, III
Orrick, Herrington & Sutcliffe, LLP
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Menlo Park, CA 94025
Telephone: (650) 614-7452

Facsimile number 10256-00453531 / (650) 614-7401

From Frank E. Scherkenbach

Re Power Integrations, Inc. v. Fairchild Semiconductor International
USDC-D. Del. – C.A. No. 04-1371 JJF

Number of pages including this page 2

Message Please see attached.

FISH & RICHARDSON P.C.

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Frederick P. Fish
1855-1930

W.K. Richardson
1859-1951

BY FACSIMILE AND U.S. MAIL
(650) 614-7401

August 11, 2006

G. Hopkins Guy, III
Orrick, Herrington & Sutcliffe, LLP
1000 Marsh Road
Menlo Park, CA 94025

Re: Power Integrations, Inc. v. Fairchild Semiconductor International
USDC-D. Del. - C.A. No. 04-1371 JJF

Dear Hop:

Thanks for your letter and voicemail of earlier today, stating that Fairchild will not call Mr. Schott as a witness at either trial and is therefore canceling his deposition on next Tuesday the 15th. We had already started our preparations but will delay those based on your representation.

It does not follow, however, that our motion on the scope of waiver is moot. Resolving that dispute is not as simple as allowing REDACTED in his continued deposition, to answer one more question. We are entitled to explore whether REDACTED has any information, from any source, relating to the validity or infringement of the patents. We are also entitled to discover any information Fairchild, and not only REDACTED personally, received on the subject matters of the opinions. Therefore, while I appreciate Fairchild reconsidering what questions REDACTED can answer, Fairchild cannot withhold other communications it received relating to the validity and infringement of the patents. These other communications include at least those documents on Fairchild's privilege log which we identified in our letter brief.

Sincerely,

Frank E. Scherkenbach

FES/cms

EXHIBIT C

ORRICK

ORRICK, HERRINGTON & SUTCLIFFE LLP
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MENLO PARK, CALIFORNIA 94025
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fax 650-614-7401
www.orrick.com

Michael John B. de Blank
(650) 614-7343
bdeblank@orrick.com

August 14, 2006

VIA FACSIMILE

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

Dear Frank:

I write in response to your letter of August 11, 2006. I am glad that we agreed that the deposition of Mr. Schott will not be taken. Concerning Power Integrations' pending motion on the scope of waiver in relation to Fairchild's reliance on the advice of its opinion counsel, we believe the matter is moot.

We have, once again, reviewed each of the documents on Fairchild's privilege document questioned by Power Integrations. The vast majority of these documents have nothing whatsoever to do with the infringement or validity of the four asserted Power Integrations patents. As you recall, Power Integrations' discovery requests were exceedingly broad and are not limited to the accused devices or the asserted patents. In order to err on the side of caution, Fairchild logged privileged documents, including documents relating to competitors other than Power Integrations. Obviously, the privilege on these documents has not been waived by Fairchild's reliance on the advice of counsel with respect to the four asserted Power Integrations patents.

Four of the documents identified by Power Integrations (nos. 213 and 417-419) identify one or more of the asserted patents by number. While we do not believe that these documents are necessarily relevant to issues of infringement or validity, we have enclosed redacted versions of these documents (removing only those portions relating to topics other than the asserted patents).

ORRICK

I hope that this resolves all outstanding issues with respect to Power Integrations' pending motion and that Power Integrations will now withdraw the motion as moot. If this is not the case, please let me know what issues you believe remain so that we can either resolve them or address them in our opposition.

Sincerely,

Bas de Blank

Encl.

cc: William J. Marsden, Jr.
Howard G. Pollack

Attorney-Client Privileged

FAX TRANSMITTAL SHEET

To: Stephen Schott
Fax #: 001-1-207-775-8026
Phone #: 001-1-207-775-8192
Date: Jan 9 , 2004
# of Pages (including cover): 47
From: SE

Hello Steve,
The attached documents are related with some products.
I think we should have a video or call conference with these documents as soon as possible. It's very urgent thing for us.

Attachements

1. USP 6,249,876
2. PDD Application(I2200306009, filed in US by [redacted] not got the filing NO)
3. Prior Art(it will also be sent by email). REDACTED

-the end-

Fairchild Confidential

Pages 1-21
Redacted

REDACTED

4526844
Derwent Accession: 2001-578802
Utility
CERTIFICATE OF CORRECTION
E/ Frequency jittering control for varying the switching frequency of a power supply
Inventor: Balakrishnan, Balu , Saratoga, CA
Djenguerian, Alex, Saratoga, CA
Lund, Leif, San Jose, CA
Assignee: Power Integrations, Inc. (OZ), San Jose, CA
Power Integrations Inc (Code: 36042)

	Publication Number	Kind	Date	Application Number	Filing Date
Main Patent	US 6249876	A	20010619	US 98192959	19981116
Priority				US 98192959	19981116

Fulltext Word Count: 5745
Post Issue Legal Status:
Calculated Expiration Date: 20181116
Certificate of Correction issued on: 20020312

Abstract:
EMI emission is reduced by jittering the switching frequency of a switched mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is connected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

5/4,LS/25
DIALOG(R)File 654:US PAT.FULL.
(c) FORMAT ONLY 2003 THE DIALOG CORP. All rts. reserv.

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4504016
Derwent Accession: 2001-388535
Utility
CERTIFICATE OF CORRECTION
E/ Off-line converter with integrated softstart and frequency jitter
Inventor: Balakirshnan, Balu, Saratoga, CA
Djenguerian, Alex, Saratoga, CA
Lund, Leif, San Jose, CA
Assignee: Power Integrations, Inc. (02), Sunnyvale, CA
Power Integrations Inc (Code: 36042)

	Publication Number	Kind	Date	Application Number	Filing Date
Main Patent	US 6229366	A	20010508	US 2000573081	20000516
Division	US 6107851	A		US 9880774	19980518
Priority				US 2000573081	20000516
				US 9880774	19980518

Fulltext Word Count: 7623

Post Issue Legal Status:
Calculated Expiration Date: 20180518
Certificate of Correction issued on: 20020129

Abstract:
A pulse width modulated switch comprises a first terminal, a second terminal, and a switch that allows a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at a control input. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency

variation signal and an oscillator that provides an oscillation signal having a frequency of that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated switch further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

Parent Case Text:
CROSS-REFERENCE TO RELATED APPLICATION
This is a Divisional of U.S. application Ser. No. 09/080,774, filed May 18, 1998, now U.S. Pat. No. 6,107,851.

5/4,LS/27
DIALOG(R)File 654:US PAT.FULL.

REDACTED

Pages 25-27
Redacted

REDACTED

Derwent Accession: 2000-578561
Utility
E/ Offline converter with integrated softstart and frequency jitter
Inventor: Balakirshnan, Balu, Saratoga, CA
Djenguerian, Alex, Saratoga, CA
Lund, Leif, San Jose, CA
Assignee: Power Integrations, Inc. (02), Sunnyvale, CA
Power Integrations Inc (Code: 36042)

	Publication Number	Kind	Date	Application Number	Filing Date
Main Patent	US 6107851	A	20000822	US 9880774	19980518
Priority				US 9880774	19980518

Fulltext Word Count: 7599
Calculated Expiration Date: 20180518

Abstract:
A pulse width modulated switch comprises a first terminal, a second terminal, and a switch that allows a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at a control input. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency of that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated switch further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

5/4,LS/34
DIALOG(R)File 654:US PAT.FULL.

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Pages 30-54
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REDACTED

2945219
Derwent Accession: 1988 361935
Utility
REASSIGNED
E/ High voltage MOS transistors
Inventor: Eklund, Klas H., Los Gatos, CA
Assignee: Power Integrations, Inc. (02), Mountain View, CA
POWER INTEGRATIONS INC (Code: 36042)

	Publication Number	Kind	Date	Application Number	Filing Date
Main Patent	US 4811075	A	19890307	US 8741994	19870424
Priority				US 8741994	19870424

Fulltext Word Count: 5543

Post Issue Legal Status:
Calculated Expiration Date: 20070424
Reassignment:
Recorded: 19950314
Action: SECURITY INTEREST
Assignor: POWER INTEGRATIONS, INC. DATE SIGNED: 02/15/1995
Assignee: IMPERIAL BANK 226 AIRPORT PARKWAY SAN JOSE, CALIFORNIA 95110
Reel: 007470
Frame: 0543
Contact: WILLIAM S. VEATCH, ESQ. COOLEY GODWARD CASTRO HUDDLESON & TATUM 5 PALO ALTO SQUARE 4TH FLOOR PALO ALTO, CA 94306

Recorded: 19960719
Action: SECURITY AGREEMENT
Assignor: POWER INTEGRATIONS, INC. DATE SIGNED: 05/22/1996
Assignee: HAMBRECHT & QUIST TRANSITION CAPITAL, INC. ONE BUSH STREET SAN FRANCISCO, CALIFORNIA 94104
Reel: 008040
Frame: 0236
Contact: HAMBRECHT & QUIST PATRICIA KOEL ONE BUSH STREET SAN FRANCISCO, CA 94104

Abstract:
An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

5/4,LS/63
DIALOG(R)File 654:US PAT.FULL.

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Pages 57-73
Redacted

Pages 1-95
Redacted

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014094588 **Image available**
WPI Acc No: 2001-578802/200165
XRPX Acc No: N01-430716
Digital frequency jittering circuit has counter coupled to oscillator and D/A converter to adjust operation of switching terminal of oscillator based on which switching frequency of generated signal is varied
Patent Assignee: POWER INTEGRATIONS INC (POWE-N
Inventor: BALAKRISHNAN B; DJENGUERIAN A; LUND L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6249876	B1	20010619	US 98192959	A	19981116	200165	B

Priority Applications (No Type Date): US 98192959 A 19981116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6249876	B1		13	G06F-001/04	

Abstract (Basic): US 6249876 B1
NOVELTY - Primary oscillator (110) which generates a signal having switching frequency, includes a frequency switching terminal coupled to D/A convertor (150). Counter (140) is coupled to oscillator and the D/A convertor to adjust the operation of switching terminal of oscillator

based on which switching frequency of generated signal is varied.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Switching frequency generating method;
(b) Power supply
USE - For varying switching frequency of a power supply.
ADVANTAGE - Spreads energy outside of the bandwidth measured by the EMI measuring equipment, as the jittering operation smears the switching frequency of power supply over a wide frequency range. Considerably reduces the average noise by changing oscillator frequency back and forth. Enables to maintain jittering operation even at high temperature by minimizing effects caused by leakage current from transistors and capacitors associated with low frequency oscillators.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of digital frequency jittering device.
Primary oscillator (110)
Counter (140)
D/A convertor (150)
pp; 13 DwgNo 1/6
Title Terms: DIGITAL; FREQUENCY; CIRCUIT; COUNTER; COUPLE; OSCILLATOR; CONVERTER; ADJUST; OPERATE; SWITCH; TERMINAL; OSCILLATOR; BASED; SWITCH; FREQUENCY; GENERATE; SIGNAL; VARY
Derwent Class: T01
International Patent Class (Main): G06F-001/04
File Segment: EPI
Manual Codes (EPI/S-x): T01-L01

1/9/56
DIALOG(R)File 351:Derwent WPI
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REDACTED

Pages 98-104
Redacted

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013406623 **Image available**
WPI Acc No: 2000-578561/200054
Related WPI Acc No: 2001-388585
XRPX Acc No: N00-428072
Pulse width modulated switch for power supply, has oscillator which outputs maximum duty cycle signal based on state of which drive circuit outputs drive signal
Patent Assignee: POWER INTEGRATIONS INC (POWE-N
Inventor: BALAKIRSHNAN B; DJENGUERIAN A; LUND L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6107851	A	20000822	US 9880774	A	19980518	200054 B

Priority Applications (No Type Date): US 9880774 A 19980518
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6107851	A		18	H03K-003/017	

Abstract (Basic): US 6107851 A
NOVELTY - An oscillator (465) generates oscillation signal whose frequency is varied depending on output of a frequency variation circuit (405). The magnitude of oscillation signal is below a variable threshold level. The oscillator also outputs maximum duty cycle signal, based on state of which a drive circuit outputs drive signal.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for regulation circuit.
USE - For power supply used in integrated electronic devices.
ADVANTAGE - Both soft start and frequency variation capabilities can be provided without increasing cost. Since number of components is reduced, cost and size of the power supply are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the circuit block diagram of the pulse width modulated switch.
Frequency variation circuit (405)
Oscillator (465)
pp; 18 DwgNo 6/9
Title Terms: PULSE; WIDTH; MODULATE; SWITCH; POWER; SUPPLY; OSCILLATOR; OUTPUT; MAXIMUM; DUTY; CYCLE; SIGNAL; BASED; STATE; DRIVE; CIRCUIT; OUTPUT; DRIVE; SIGNAL
Derwent Class: U22
International Patent Class (Main): H03K-003/017
File Segment: EPI
Manual Codes (EPI/S-X): U22-A; U22-A01; U22-B; U22-E01A

1/9/64
DIALOG(R)File 351:Derwent WPI
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Page 105

Pages 106-134
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007728003 **Image available**
WPI Acc No: 1988-361935/198851
XRPX Acc No: N88-274124
High-voltage MOS transistor with IGFET - has double-sided junction gate FET on same chip with field effect gate pinching-off extended drain region
Patent Assignee: POWER INTEGRATIONS (POWE-N); POWER INTEGRATIONS INC (POWE-N
Inventor: EKLUND K H
Number of Countries: 003 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 295391	A	19881221	EP 88106404	A	19880421	198851	B
JP 63314869	A	19881222	JP 88100015	A	19880422	198906	
US 4811075	A	19890307	US 8741994	A	19870424	198912	
EP 295391	B	19910130				199105	
DE 3861707	G	19910307				199111	
JP 8172184	A	19960702	JP 88100015	A	19880422	199636	
			JP 95196950	A	19880422		

Priority Applications (No Type Date): US 8741994 A 19870424
Cited Patents: 1.Jnl.Ref; EP 114435; EP 179693
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 295391	A	E	9		
US 4811075	A		6		
JP 8172184	A		7	H01L-029/78	Div ex application JP 88100015

Abstract (Basic): EP 295391 A

A p-channel high-voltage MOS transistor a p-type silicon substrate (11) with a pair of pockets (35,36) of p+ conductivity adjoining the substrate surface. A source contact (31) is connected to one pocket and a drain contact (32) is connected to the other pocket. An extended drain region (37) of p-type material extends laterally on either side from the drain contact pocket.

A top layer (39) of n-material is ion- through the same window of the mask as the extended drain region to cover an intermediate part of it. The top layer material and the substrate are subjected to a reverse-bias voltage. The polysilicon gate (34) on the insulating SO2 layer (12) forms a channel laterally between the source contact pocket and extended drain region, and controls by field-effect the flow of current under it through the channel.

ADVANTAGE - Highly efficient MOS transistor is provided which is compatible with five volt logic and has figure of merit Ron by A of two ohms mm square.

2/5

Abstract (Equivalent): EP 295391 B

A high voltage MOS transistor (10; 30) comprising: a semiconductor substrate (11) of a first conductivity type having a surface, a pair of laterally spaced pockets (21, 24) of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface, a source contact (14) connected to one pocket (21), a drain contact (16, 32) connected to the other pocket (24), a drain region (26) of the second conductivity type extending laterally from the drain contact pocket (24) to a surface-adjoining position, a surface-adjoining layer (27) of material of the first conductivity type on top of an intermediate portion of the drain region (26) between the drain contact pocket (24) and the surface-adjoining position, said substrate (11) being subject to application of a reverse-bias voltage, an insulating layer (12) on the surface of the substrate (11) and covering at least that portion between the source contact pocket (21) and the nearest surface-adjoining position of the drain region (26), and a gate electrode (17) on the insulating layer (12) and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket (21) and the nearest surface-adjoining position of the drain region (26), said gate electrode (17) controlling by field-effect the flow of current thereunder through the channel, characterized in that said drain region (26) is an extended one extending laterally each way from the drain contact pocket to the surface-adjoining positions, and said surface-adjoining layer (27) extends between the drain contact pocket (24) and the surface-adjoining positions and is physically connected to said substrate (11;33) so that biasing said substrate (11) means also biasing said surface-adjoining layer (27). (9pp)

Abstract (Equivalent): US 4811075 A

The insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor.

An extended drain region is formed on top of a substrate of opposite conductivity-type material.

A top layer of material having a conductivity-type opposite that of he extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region.

This top layer covers only an intermediate portion of the extended drain whic has ends contacting a silicon dioxide layer.

The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

ADVANTAGE - Increased efficiency.

(6pp Dwg.No. 1/5)

Title Terms: HIGH; VOLTAGE; MOS; TRANSISTOR; IGFET; DOUBLE; SIDE; JUNCTION; GATE; FET; CHIP; FIELD; EFFECT; GATE; PINCH; EXTEND; DRAIN; REGION

Derwent Class: U12; U13

International Patent Class (Main): H01L-029/78

International Patent Class (Additional): H01L-027/08

File Segment: EPI

Manual Codes (EPI/S-X): U12-D02A; U12-E01; U13-D02

REDACTED

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NO	"Power Integrations" PAT NO	"Power Integrations" Title	Notes

REDACTED

45	US6249876	Frequency jittering control for sr
47	US6229366	Off-line converter with integrate

REDACTED

80 US4811075 High voltage MOS transistors

REDACTED

REDACTED is doing analysis

Related to one that

REDACTED will do

REDACTED

Confirm REDACTED has

NO PAT NO

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Title

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Frequency jittering control for varying the switching frequency of a power supply
Switched mode power supply responsive to voltage across energy transfer element
Off-line converter with integrated softstart and frequency jitter

Offline converter with integrated softstart and frequency jitter

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No	US patent
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No	US patent	Comments
1	US4811075	Already reviewed with REDACTED for SDG-3 and SDG-4 and determined not to be a problem. Needs to be reduced to writing. Communicated with REDACTED he will implement.

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CERTIFICATE OF SERVICE

I hereby certify that on the 22nd day of August, 2006, the attached **REDACTED PUBLIC VERSION OF DEFENDANTS' ANSWERING BRIEF IN RESPONSE TO PLAINTIFF'S MOTION TO COMPEL PRIVILEGED INFORMATION** was served upon the below-named counsel of record at the address and in the manner indicated:

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